respectfully submits that none of the base claims now pending in the application are anticipated under the provisions of 35 U.S.C. § 102. As such and for at least the reasons set forth herein, the Applicant also submits that the claims dependent upon the base claims are also not anticipated under the provisions of 35 U.S.C. § 102 and are patentable thereunder.

As such, the Applicant respectfully submits that the basis for the Examiner's objections to Applicant's claims 11-13, 15, and 21 has been removed. Therefore it is respectfully requested that these objections be withdrawn.

Rejections

A. 35 U.S.C. § 102

The Examiner rejected claims 1-10, 14 and 16-20 under 35 U.S.C. § 102(b) as being anticipated by Panahi et al. (hereinafter Panahi), U.S. Patent 6,272,130. The rejection is respectfully traversed.

Claims 1 and 16

The Examiner alleges that regarding claims 1 and 16, referring to figures 11 and 12, Panahi teaches apparatus for providing synchronization signals to a telecommunications network comprising: a central synchronization management unit (1100) (Fig. 11) for distributing synchronization signals (from col. 12, line 38 to col. 13, line 65), and a synchronization distribution unit (1200) (Fig. 12) connected to receive synchronization signals from the central synchronization management unit (1100) and to distribute the signals to at least one network element (1260) (i.e., data sink) (from col. 13, line 66 to col. 14, line 36). The Applicant respectfully disagrees.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrik Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)) (emphasis added).

The Panahi reference fails to teach or disclose at least the invention as recited in Applicant's claim 1 as follows:

> "Apparatus for providing synchronization signals to a telecommunications network comprising:
> a central synchronization management unit for distributing synchronization signals; and
> a synchronization distribution unit connected to receive synchronization signals from the central synchronization management unit and to distribute the signals to at least one network element." (emphasis added).

The Applicant's invention is directed to several embodiments of synchronization systems, wherein synchronization and management signals are carried over links between a central synchronizing management unit and each synchronizing distribution unit, and between each synchronizing distribution unit and each network element. (See Applicant's Specification, page 4, lines 21-24). The Applicant further teaches "The distributed architecture of the present invention, an architecture that distributes synchronization and management signals to synchronization distribution units which, in turn, distribute signals to network elements, reduces the number of links required for the distribution of these signals. That is, each synchronization distribution unit acts as a concentrator, preferably communicating with a plurality of network elements and thereby limiting the number of direct links to a central synchronization management unit." (See Applicant's Specification, page 6, lines 23-29).

There is absolutely no teaching or disclosure in Panahi for "a central synchronization management unit for distributing synchronization signals" and "a synchronization distribution unit connected to receive synchronization signals from the central synchronization management unit and to distribute the signals to at least one network element" as claimed in the Applicant's claim 1. The Examiner alleges that, in Panahi, the multiplexer 1100 teaches the central synchronization management unit of the Applicant's invention and that the

demultiplexer 1200 teaches the synchronization distribution unit of the Applicant's invention. The Applicant respectfully disagrees.

Panahi teaches a time-division multiplexer-demultiplexer system. The invention of Panahi teaches:

> "Second, the data source block 1110 generates a synchronous signal at block 1112. In the illustrated example the synchronous data is T1 data, which is a standard telephony signal with very stringent specific frequency and timing tolerances/requirements. The fact that the T1 signal has the most stringent frequency and timing requirements results in the T1 data clock being used as the master clock for the demultiplexer 1200, as described below." (See Panahi, col. 12, lines 56-63).

> "Functionally speaking, the time division demultiplexer 1200 is the mirror image of the time division multiplexer 1100. Thus, for whatever "processing" is done with respect to the individual data streams by the time division multiplexer 1100, there is a corresponding "deprocessing" performed by the time division demultiplexer 1200. For this reason, the discussion of the time division demultiplexer 1200 illustrated in FIG. 12 is less detailed than the discussion of the time division multiplexer 1100 illustrated in FIG. 11.
>
> The demultiplexer 1210 receives the data streams transmitted over the communication medium from the multiplexer 1150. The demultiplexer 1210 deserializes the data and decodes from the 10B/12B encoding format. The deserialized data streams are then fed to the traffic desynchronizer block 1220 which restores the original timing of the data streams. This is done in conjunction with a clock recovery circuit 1212 which is coupled to an intelligent timing/clock recovery clock generator circuit 1230. Again, the clock generator circuit 1230 receives an input from the clock resynchronization circuit 1241, which is coupled to the T1 data stream." (See Panahi, col. 14, lines 6-27).

The time-division multiplexer-demultiplexer system taught in Panahi does not distribute any synchronization signals. Instead, a data source within a data source block generates parallel data having a clock, in one case a T1 clock, which is used by the demultiplexer for deprocessing. That is, for whatever processing is done with respect to the individual data streams by the time division multiplexer, there is a corresponding deprocessing performed by the

demultiplexer. (See Panahi, col. 14, lines 6-12). The demultiplexer simply restores the timing of the original data to perform deprocessing functions. The multiplexer of Panahi does not perform the function of "a central synchronization management unit for distributing synchronization signals" as claimed in the Applicant's claim 1 and the demultiplexer does not perform the function of "a synchronization distribution unit connected to receive synchronization signals from the central synchronization management unit" as claimed in the Applicant's claim 1.

Furthermore, the demultiplexer of Panahi does not teach or disclose or perform "a synchronization distribution unit connected to receive synchronization signals from the central synchronization management unit and to distribute the signals to at least one network element" as claimed in the Applicant's claim 1. The Examiner alleges that, in Panahi, the demultiplexer 1100 performs the function of distributing the synchronization signals from the central synchronization unit to at least one network unit (i.e., data sink 1260). The Applicant respectfully disagrees.

Panahi teaches:

> "The demultiplexer 1210 receives the data streams transmitted over the communication medium from the multiplexer 1150. The demultiplexer 1210 deserializes the data and decodes from the 10B/12B encoding format. The deserialized data streams are then fed to the traffic desynchronizer block 1220 which restores the original timing of the data streams. This is done in conjunction with a clock recovery circuit 1212 which is coupled to an intelligent timing/clock recovery clock generator circuit 1230. Again, the clock generator circuit 1230 receives an input from the clock resynchronization circuit 1241, which is coupled to the T1 data stream.
>
> The post processor block performs a further demultiplexing function. This demultiplexing function corresponds to the multiplexing function performed by the data/traffic processor/analyzer block 1120. The post processor block 1250 also performs digital to analog conversion for the real time audio/visual signal generated at the block 1111. The data streams from the post processor 1250 are then fed to the data sync 1260, where they are then ready for use." (See Panahi, col. 14, lines 16-36).

Panahi teaches that the data streams from the post processor are fed forward to a data sync. There is absolutely no teaching of a synchronization distribution unit for distributing synchronization signals from a central synchronization management unit to at least one network element as taught and claimed by the Applicant. The Applicant submits that even if the demultiplexer of Panahi could be equated to the synchronization distribution unit of the Applicant's invention (which the Applicant submits that no such parallel can be made) the demultiplexer of Panahi does not and cannot perform the function of distributing synchronization signals to at least one network element as taught and claimed by the Applicant. The demultiplexer of Panahi simply forwards signals processed by the demultiplexer to be used by the data sink. As such, and for at least the reasons stated above, the Applicant submits that the teachings and disclosure of Panahi do not anticipate the Applicant's invention, at least with respect to claim 1.

Therefore, the Applicant submits that claim 1 is not anticipated by the teachings of Panahi and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claim 16 recites similar relevant features as recited in claim 1. As such, the Applicant submits that independent claim 16 is also not anticipated by the teachings of Panahi and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 2-10, 14 and 16-20 depend either directly or indirectly from claims 1 and 16 and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicant submits that dependent claims 2-10, 14 and 16-20 are also not anticipated by the teachings of Panahi. Therefore the Applicant submits that dependent claims 2-10, 14 and 16-20 also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

Applicant's Note

The Applicant would like to thank the Examiner for his suggestions regarding the allowability of claims 11-13, 15 and 21, but at this time the Applicant believes all of the claims in this application to be allowable. The Applicant reserves the right to individually argue the patentability of each, independent and dependent claim at a latter time.

Conclusion

Thus the Applicant submits that none of the claims, presently in the application, are anticipated under the provisions of 35 U.S.C. § 102. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

E/Wall

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